AMENDMENT

In the claims:

1. (currently amended) A pipeline accelerator, comprising:

a communication bus; and

a plurality of pipeline units each coupled to the communication bus and each comprising a respective hardwired-pipeline circuit that is coupled to receive and is operable in response to a respective clock signal that is unsynchronized~~operable simultaneously~~ with ~~and asynchronously relative to~~ the respective clock signal received by at least one of the other hardwired-pipeline circuits.

2.(original) The pipeline accelerator of claim 1 wherein each of the pipeline units comprises:

a respective memory coupled to the hardwired-pipeline circuit; and

wherein the hardwired-pipeline circuit is operable to,

receive data from the communication bus,

load the data into the memory,

retrieve the data from the memory,

process the retrieved data, and

drive the processed data onto the communication bus.

3. (original) The pipeline accelerator of claim 1 wherein each of the pipeline units comprises:

a respective memory coupled to the hardwired-pipeline circuit; and

wherein the hardwired-pipeline circuit is operable to,

receive data from the communication bus,

process the data,

load the processed data into the memory,

retrieve the processed data from the memory, and

load the retrieved data onto the communication bus.

4. (currently amended) A pipeline accelerator, comprising:

a communication bus;

a plurality of pipeline units each coupled to the communication bus and each comprising a respective hardwired-pipeline circuit; and

wherein each of the hardwired-pipeline circuits is disposed on a respective field-programmable gate array die.

5. (original) The pipeline accelerator of claim 1, further comprising:

a pipeline bus; and

a pipeline-bus interface coupled to the communication bus and to the pipeline bus.

6. (original) The pipeline accelerator of claim 1, further comprising:

wherein the communication bus comprises a plurality of branches, a respective branch coupled to each pipeline unit; and

a router coupled to each of the branches.

7. (original) The pipeline accelerator of claim 1, further comprising:

wherein the communication bus comprises a plurality of branches, a respective branch coupled to each pipeline unit;

a router coupled to each of the branches;

a pipeline bus; and

a pipeline-bus interface coupled to the router and to the pipeline bus.

8. (original) The pipeline accelerator of claim 1, further comprising:

wherein the communication bus comprises a plurality of branches, a respective branch coupled to each pipeline unit;

a router coupled to each of the branches;

a pipeline bus;

a pipeline-bus interface coupled to the router and to the pipeline bus; and

a secondary bus coupled to the router.

9. (original) The pipeline accelerator of claim 1 wherein:

the communication bus is operable to receive data addressed to one of the pipeline units; and

the one pipeline circuit is operable to accept the data; and

the other pipeline circuits are operable to reject the data.

10. (original) The pipeline accelerator of claim 1, further comprising:

wherein the communication bus comprises a plurality of branches, a respective branch coupled to each pipeline unit;

a router coupled to each of the branches and operable to,

receive data addressed to one of the pipeline units, and

provide the data to the one pipeline unit via the respective branch of the communication bus.

11. (currently amended) A computing machine, comprising:

a processor;

a pipeline-accelerator configuration registry operable to store hardwired-pipeline-configuration information;

~~a pipeline bus coupled to the processor and operable to carry data and hardwired-pipeline-configuration information; and~~

a pipeline accelerator comprising,

a communication bus,

a pipeline-bus interface coupled to~~between the pipeline bus and~~ the communication bus, and

a plurality of pipeline units each coupled to the communication bus and each comprising a respective hardwired-pipeline circuit; and~~.~~

a pipeline bus coupled to the processor, the registry, and the pipeline-bus interface of the pipeline accelerator, the pipeline bus operable to carry data between the

processor and the pipeline accelerator and to carry the hardwired-pipeline-configuration information from the registry to the pipeline accelerator.

12. (original) The computing machine of clam 11 wherein:

the processor is operable to generate a message that identifies one of the pipeline units and to drive the message onto the pipeline bus;

the pipeline-bus interface is operable to couple the message to the communication bus;

the pipeline units are each operable to analyze the message;

the identified pipeline unit is operable to accept the message; and

the other pipeline circuits are operable to reject the message.

13. (original) The computing machine of claim 11, further comprising:

wherein the communication bus comprises a plurality of branches, a respective branch coupled to each pipeline unit;

wherein the processor is operable to generate a message that identifies one of the pipeline units and to drive the message onto the pipeline bus; and

a router coupled to each of the branches and to the pipeline-bus interface and operable to receive the message from the pipeline-bus interface and to provide the message to the identified pipeline unit.

14. (original) The computing machine of claim 11, further comprising:

wherein the communication bus comprises a plurality of branches, a respective branch coupled to each pipeline unit;

a secondary bus; and

a router coupled to each of the branches, to the pipeline-bus interface, and to the secondary bus.

15. (currently amended) A method, comprising:

sending via a communication bus first data and second data to first and second ones, respectively, of a plurality of pipeline units, each pipeline unit including a respective hardwired pipeline;

processing the first data with the first pipeline unit in response to a first clock signal; and

processing the second data with the second pipeline unit in response to a second clock signal~~asynchronously with respect to the first pipeline unit~~ and while the first pipeline unit is processing the first data, the second clock signal being unsynchronized to the first clock signal.

16. (previously pending) The method of claim 15 wherein sending the data comprises:

sending the data to a router; and

providing the first data to the first pipeline unit with the router via a respective first branch of the communication bus.

17. (previously pending) The method of claim 15 wherein sending the first data comprises sending the first data to the first pipeline unit with a processor.

18. (previously pending) The method of claim 15 wherein sending the first data comprises sending the first data to the first pipeline with a third of the plurality of pipeline units.

19. (previously pending) The method of claim 15, further comprising driving the processed first data onto the communication bus with the first pipeline unit.

20. (previously pending) The method of claim 15 wherein processing the first data with the first pipeline unit comprises:

receiving the first data from the communication bus with a hardwired-pipeline circuit,

loading the first data into a memory with the hardwired-pipeline circuit,

retrieving the first data from the memory with the hardwired-pipeline circuit, and

processing the retrieved first data with the hardwired-pipeline circuit.

21. (previously pending) The method of claim 15, further comprising:

wherein processing the first data with the first pipeline unit comprises,

receiving the first data from the communication bus with a hardwired-pipeline circuit,

processing the received first data with the hardwired-pipeline circuit, and

loading the processed first data into a memory with the hardwired-pipeline circuit; and

retrieving the processed first data from the memory and driving the processed first data onto the communication bus with the hardwired-pipeline circuit.

22. (currently amended) The method of claim 15, further comprising:

generating a message that includes the first data and that identifies the first pipeline unit as a recipient of the message; and

wherein sending the first data to the first pipeline unit comprises determining from the message that the first pipeline is a recipient of the message.

23. (previously pending) A computing machine, comprising:

a memory operable to store program instructions;

a program-instruction bus coupled to the memory;

a pipeline bus that is separate from the program-instruction bus;

a processor coupled to the program-instruction bus and to the pipeline bus and operable to retrieve the program instructions from the memory via the program-instruction bus and to execute the program instructions; and

a pipeline accelerator inoperable to communicate directly with the program-instruction bus, the pipeline accelerator comprising,

a communication bus,

a pipeline-bus interface coupled between the pipeline bus and the communication bus, and

a plurality of pipeline units each coupled to the communication bus and each comprising a respective hardwired-pipeline circuit.

24. (previously pending) A method, comprising:

retrieving with a processor program instructions from a memory via a program-instruction bus;

executing the instructions with the processor; and

transferring information between the processor and pipeline units of a pipeline accelerator via a pipeline bus that is separate from the program-instruction bus, the pipeline accelerator inoperable to directly communicate with the program-instruction bus.

25. (previously pending) The method of claim 24, further comprising:

wherein the information comprises data;

wherein transferring the information comprises sending the data from the processor to the pipeline units; and

processing the data with the pipeline units.

26. (previously pending) The method of claim 24, further comprising:

wherein the information comprises data;

wherein transferring the information comprises sending the data from the pipeline units to the processor; and

processing the data with the processor.

27. (previously pending) The method of claim 24 wherein the information comprises addresses of the pipeline units.

28. (new) The computing machine of claim 11 wherein the pipeline bus is coupled to the pipeline-accelerator configuration registry via the processor.

29. (new) The pipeline accelerator of claim 1 wherein at least one of the respective hardwired-pipeline circuits is disposed on a field-programmable gate array.

30. (new) The pipeline accelerator of claim 1 wherein at least one of the respective hardwired-pipeline circuits is disposed on an application-specific integrated circuit.

31. (new) The pipeline accelerator of claim 1 wherein:

at least one of the respective hardwired-pipeline circuits is disposed on an application-specific integrated circuit; and

at least one of the respective hardwired-pipeline circuits is disposed on a field-programmable gate array.

32. (new) The computing machine of claim 11 wherein at least one of the pipeline units comprises a field-programmable gate array.

33. (new) The computing machine of claim 11 wherein at least one of the pipeline units comprises an application-specific integrated circuit.

34. (new) The computing machine of claim 11 wherein:

at least one of the pipeline units comprises a field-programmable gate array; and

at least one of the pipeline units comprises an application-specific integrated circuit.